FIELD EMISSION DISPLAY HAVING REDUCED
POWER REQUIREMENTS AND METHOD

TECHNICAL FIELD

5   This invention relates to field emission displays, and, more particularly, to a method and apparatus for reducing power consumption in field emission displays.

BACKGROUND OF THE INVENTION

Figure 1 is a simplified side cross-sectional view of a portion of a display 10 including a faceplate 20 and a baseplate 21, in accordance with the

10   prior art. Figure 1 is not drawn to scale. The faceplate 20 includes a transparent viewing screen 22, a transparent conductive layer 24 and a cathodoluminescent layer 26. The transparent viewing screen 22 supports the layers 24 and 26, acts as a viewing surface and forms a hermetically sealed package between the viewing screen 22 and the baseplate 21. The viewing screen 22 may be formed

15   from glass. The transparent conductive layer 24 may be formed from indium tin oxide. The cathodoluminescent layer 26 may be segmented into pixels yielding different colors to provide a color display 10. Materials useful as cathodoluminescent materials in the cathodoluminescent layer 26 include Y_2O_3:Eu (red, phosphor P-56), Y_3(Al, Ga)$_5O_{12}$:Tb (green, phosphor P-53) and

20   Y_2(SiO$_5$):Ce (blue, phosphor P-47) available from Osram Sylvania of Towanda PA or from Nichia of Japan.

The baseplate 21 includes emitters 30 formed on a surface of a substrate 32. The substrate 32 is coated with a dielectric layer 34 that is formed, in accordance with the prior art, by deposition of silicon dioxide via a

25   conventional TEOS process. The dielectric layer 34 is formed to have a thickness that is approximately equal to or just less than a height of the emitters 30. This thickness may be on the order of 0.4 microns, although greater or lesser thicknesses may be employed. A conductive extraction grid 38 is formed on the

dielectric layer 34. The extraction grid 38 may be, for example, a thin layer of polycrystalline silicon. An opening 40 is created in the extraction grid 38 having a radius that is also approximately the separation of the extraction grid 38 from the tip of the emitter 30. The radius of the opening 40 may be about 0.4 microns,

5   although larger or smaller openings 40 may also be employed.

In operation, signals coupled to the emitter 30 allow electrons to flow to the emitter 30. Intense electrical fields between the emitter 30 and the extraction grid 38 then cause field emission of electrons from the emitter 30. A positive voltage, ranging up to as much as 5,000 volts or more but generally

10   2,500 volts or less, is applied to the faceplate 20 via the transparent conductive layer 24. The electrons emitted from the emitter 30 are accelerated to the faceplate 20 by this voltage and strike the cathodoluminescent layer 26. This causes light emission in selected areas known as pixels, *i.e.*, those areas adjacent to the emitters 30, and forms luminous images such as text, pictures and the like.

15   Figure 2 is a simplified plan view showing rows 42 and columns 44 of the emitters 30 and the openings 40 of Figure 1, according to the prior art. The columns 44 are divided into top columns 44a and bottom columns 44b, as may be seen in Figure 2. Top 46a and bottom 46b column driving circuitry is coupled to the top 44a and bottom 44b columns, respectively. A row driving

20   circuit 48 is coupled to odd rows 42a and even rows 42b. The rows 42 are formed from strips of the extraction grid 38 that are electrically isolated from each other. The columns 44a and 44b are formed from conductive strips that are electrically isolated from each other and that electrically interconnect groups of the emitters 30.

25   By biasing a selected one of the rows 42 to an appropriate voltage and also biasing a selected one of the columns 44 to a voltage that is about forty to eighty volts more negative than the voltage applied to the selected row 42, the emitter or emitters 30 located at an intersection of the selected row 42 and column 44 are addressed. The addressed emitter or emitters 30 then emit

electrons that travel to the faceplate 20, as described above with respect to Figure 1.

Conventional circuitry for driving emitters 30 in field emission displays 10 enables each column 44 once per row address interval and disables 5 each column 44 once per row address interval. The columns 44 present a capacitive load C. Charging and discharging of the capacitance C consumes power in proportion to fCV^2, where f represents the frequency of charging and discharging the column 44 and V represents the voltage to which the columns 44 are charged. Charging and discharging of the columns 44 in order to drive the 10 emitters 30 forms a major component of the electrical power consumed by the display 10. As a result, reducing the frequency f, the capacitance C or the voltage V can significantly reduce the electrical power required to operate the display 10. Displays 10 requiring less electrical power are currently in demand.

There is therefore need for techniques and apparatus that reduce the 15 amount of electrical power required in order to operate field emission displays.

SUMMARY OF THE INVENTION

In one aspect, the present invention includes a field emission display having a substrate and a plurality of emitters formed on the substrate. Each of the emitters is formed on one of a plurality of emitter conductors that is 20 also a row or a column of the display. The display also includes a porous dielectric layer formed on the substrate and the columns. The porous dielectric layer has an opening formed about each of the emitters and has a thickness substantially equal to a height of the emitters above the substrate. The porous dielectric layer is preferably formed by oxidation of porous polycrystalline 25 silicon. The display further includes an extraction grid formed substantially in a plane defined by respective tips of the plurality of emitters. The extraction grid has an opening surrounding each tip of a respective one of the emitters. The display additionally includes a cathodoluminescent-coated faceplate having a

planar surface formed parallel to and near the plane of tips of the plurality of emitters.

The porous dielectric results in the emitter conductors having reduced capacitance C compared to prior art dielectric layers. Charging and discharging of the emitter conductors in order to drive the emitters forms a major component of the electrical power consumed by the display. By reducing the capacitance of the emitter conductors, the display is able to form luminous images, such as text and the like, while dissipating reduced electrical power.

In another aspect of the present invention, tips of the emitters are formed from a material having a work function less than four electron volts. The voltage needed in order to drive the emitters, and hence the voltage used to charge and discharge the columns, is proportional to a turn-on voltage for the emitters. Emitters having reduced turn-on voltage draw less electrical power. As a result, baseplates with emitters having low work function tips are able to form luminous images while dissipating reduced electrical power compared to conventional displays.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified side cross-sectional view of a portion of a display including a faceplate and a baseplate, in accordance with the prior art.

Figure 2 is a simplified plan view showing rows and columns of the emitters of Figure 1, in accordance with the prior art.

Figure 3 is a simplified flowchart of a process for forming a dielectric having a reduced relative dielectric constant ε_R, in accordance with embodiments of the present invention.

Figure 4 is a simplified side view of an emitter having a body formed of high resistivity material and a tip formed of a low work function material, in accordance with embodiments of the present invention.

Figure 5 is a simplified flowchart of a process for forming emitters having reduced work function and integral ballast resistors, in accordance with embodiments of the present invention.

Figures 6A-6G show the baseplate at various stages in the process 5 of emitter formation, in accordance with embodiments of the present invention.

Figure 7 is a simplified block diagram of a computer including a field emission display, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 3 is a simplified flowchart of a process 75 for forming a 10 dielectric layer 34' (not shown in Figure 3) having a reduced relative dielectric constant ε_R, relative to the prior art, in accordance with embodiments of the present invention. The process 75 begins with a step 77 of forming emitter conductors defining columns 44 (Figure 2) on the substrate 32 (Figure 1). In a step 79, a silicon layer (not shown) is formed on the substrate 32 and on the 15 emitter conductors/columns 44 by conventional processes. In one embodiment, the step 79 includes forming the silicon layer by conventional deposition of polysilicon.

In a step 81, the silicon layer is made porous. In one embodiment, the step 81 includes forming voids or pores (not shown) in an n-type silicon layer 20 by a process similar to that described in "Formation Mechanism of Porous Silicon Layers Obtained by Anodization of Monocrystalline n-type Silicon in HF Solutions" by V. Dubin, Surface Science 274 (1992), pp. 82-92. In one embodiment, a current density of between 5 and 40 mA/cm^2 is employed together with 12-24% HF. In general, increasing N_D (silicon donor 25 concentration), HF concentration or anodization current density provides larger pores.

In another embodiment, the step 81 includes forming voids or pores in a p-type silicon layer by a process similar to that described in "On the Morphology of Porous Silicon Layers Obtained by Electrochemical Method" by

G. Graciun et al., International Semiconductor Conference CAS '95 Proceedings (IEEE Catalog No. 95TH8071) (1995), pp. 331-334. In one embodiment, a current density of between 1.5 and 30 mA/cm^2 is employed together with either 36 weight % HF-ethanol 1:1 or 49 weight % HF-ethanol 1:3.

5   In one embodiment, the silicon layer is anodized or etched until a porosity of greater than 50% is achieved, *i.e.*, more than one-half of the volume of the silicon layer is converted to pores or voids. In another embodiment, the silicon layer is anodized or etched until a porosity of greater than 75% is achieved.

10   In a step 83, the porous silicon layer is oxidized. In one embodiment, the oxidation of the step 83 is carried out by conventional thermal oxidation at a temperature in excess of 950 to 1,000°C. In another embodiment, an inductively-coupled oxygen-argon mixed plasma is employed for oxidizing the silicon layer, as described in "Low-Temperature Si Oxidation Using Inductively Coupled Oxygen-Argon Mixed Plasma" by M. Tabakomori et al.,

15 Jap. Jour. Appl. Phys., Part 1, Vol. 36, No. 9A (Sep. 1997), pp. 5409-5415. In yet other embodiments, electron cyclotron resonance nitrous oxide plasma is employed for oxidizing the silicon, as described in "Oxidation of Silicon Using Electron Cyclotron Resonance Nitrous Oxide Plasma and its Application to

20 Polycrystalline Silicon Thin Film Transistors", J. Lee et al., Jour. Electrochem. Soc., Vol. 144, No. 9 (Sep. 1997), pp. 3283-3287 and "Highly Reliable Polysilicon Oxide Grown by Electron Cyclotron Resonance Nitrous Oxide Plasma" by N. Lee et al., IEEE El. Dev. Lett., Vol. 18, No. 10 (Oct. 1997), pp. 486-488. Plasma oxidation allows the temperature of the baseplate 21 (Figure 1)

25 to be as low as 450-500°C during the step 83.

Oxidation of the porous silicon layer results in the porous silicon dioxide layer 34' (not shown in Figure 3), having a porosity that is related to that of the porous silicon layer. One volume of silicon oxidizes to provide approximately 1.55 volumes of silicon dioxide. Accordingly, a silicon layer

30 having 50% voids will, after complete oxidation, result in the porous silicon

dioxide layer 34' having approximately 22.5% voids (ignoring any expansion of the porous silicon dioxide layer 34' in the vertical direction during oxidation). Similarly, a silicon layer having 75% voids will, after complete oxidation, result in the porous silicon dioxide layer 34' having approximately 61.5% voids. Either

5 of these examples will result in the porous silicon dioxide layer 34' having a relative dielectric constant ε_R that is substantially reduced compared to a dielectric layer 34 formed from silicon dioxide incorporating no voids ($\varepsilon_R \cong 3.9$).

In one embodiment, a relative dielectric constant ε_R of less than 3 is provided, corresponding to a void content of about 25% in the porous silicon

10 dioxide layer 34'. In another embodiment, a relative dielectric constant ε_R of less than 1.6 is provided, corresponding to a void content of about 60% in the porous silicon dioxide layer 34'. In some embodiments, the porous silicon dioxide layer 34' forms a series of columnar spacers.

In an optional step 85, the porous silicon dioxide layer 34' is

15 planarized. The step 85 may include conventional chemical-mechanical polishing, or may include formation of a layer of dielectric material having planarizing properties (e.g., conventional TEOS deposition). In a step 87, the extraction grid 38 is formed on the porous silicon dioxide layer 34' using conventional techniques and is etched to provide the rows 42 (Figure 2).

20 Although the field emission display is described as having emitters arranged in columns and the extraction grid arranged in rows, it will be understood that the emitters alternatively may form rows and the extraction grid may form columns. The process 75 then ends.

Figure 4 is a simplified side view of an emitter 30' having an

25 emitter body 30A formed of high resistivity material and an emitter tip 30B formed of a low work function material, in accordance with embodiments of the present invention. The emitter body 30A is formed on one of the columns 44 of Figure 2. Advantages to forming the emitter body 30A from a high resistivity material include current limiting, and equalizing the current drawn by the

30 emitters 30' despite the emitters 30' having different turn-on voltages. Current

limiting also obviates catastrophic failure of the display 10 (Figure 1) in the event that one or more emitters 30' become short-circuited to the extraction grid 38. In one embodiment, resistance values for the emitter body 30A may fall into the range of 4 MΩ to 40 MΩ for conventional drive voltages V and may be less if

5   the turn-on voltage for the emitter 30' is reduced. In one embodiment, the emitters 30' have emitter bodies 30A formed from material having a resistivity ρ of ca. 10^2-10^3 Ω-cm and emitter tips 30B formed from materials having a work function ϕ or electron affinity χ of less than four eV, or even three eV or less.

Advantages to forming emitters 30' to have tips 30B formed from a

10   metal having a low work function ϕ, or a semiconductor having a low electron affinity χ, include reduced turn-on voltage for the emitter 30'. As a result, the emitters 30' do not require as large a voltage V in order to be able to bombard the faceplate 20 with sufficient electrons to form the desired images. Power consumption for the display 10 is then reduced.

15   Representative values for work functions ϕ or electron affinities χ for several materials are summarized below in Table I. Measured or achieved work functions ϕ/ electron affinities χ depend strongly on surface treatment and surface contamination and may vary from the values given in Table I.

Table I. Metal work functions φ and semiconductor electron affinities χ for selected materials.

φ or χ (eV)	Material
4.3	W
4.05*	Si (χ)
3.6/3.7*	SiC (χ)
3.6	Zr
3.3	La
3-3.3	Zn
2.9	TiN
2.8	LaB_6
2.6	Ce
1.8-2.2	Ba
1.4**	C (diamond, χ)
0.9-4.05	Silicon oxycarbide (projected, χ)

* depending on surface treatment.
** diamond can manifest different values, including negative values.

Figure 5 is a simplified flowchart of a process 100 for forming the emitters 30' of Figure 4, in accordance with embodiments of the present invention. Figures 6A-6G show the baseplate 21 at various stages in the formation of the emitters 30 or 30', in accordance with embodiments of the present invention. In one embodiment, the process 100 results in emitters 30' having tips 30B providing reduced work function φ and emitter bodies 30A providing integral ballast resistors. In another embodiment, the process 100 results in emitters 30 that are formed after the porous silicon dioxide layer 34 is formed.

Figure 6A shows a conductor 90 forming the columns 44 (Figure 2), the dielectric layer 34 or the porous silicon dioxide layer 34' and the extraction grid 38, which were previously formed on the substrate 32. The process 100 begins with a step 102 of forming the openings 40 in the extraction grid 38 (Figure 6B). The openings 40 may be formed by conventional lithography and etching. In a step 104, the dielectric layer 34 or 34' is etched to

expose the conductor 90 (Figure 6C). The step 104 may use conventional wet chemical etching (*e.g.*, etching using buffered oxide etch, a standard HF solution) to provide a curved edge profile, shown as a solid trace in Figure 6C, or may use reactive ion etching to provide a vertical edge profile, shown as a dashed trace in

5 Figure 6C.

In a step 106, a sacrificial layer 107 (Figure 6D) is formed. The sacrificial layer 107 is formed on the extraction grid 38 but not on the conductor 90. In one embodiment, the sacrificial layer 107 is formed by evaporation of, *e.g.*, nickel, from a point source such as an electron beam evaporator, so that the

10 nickel atoms approach the extraction grid 38 at an angle of ca. 75° or more from a normal (see direction arrow 107') to the extraction grid 38, causing interiors of the openings 40 to be shadowed from the incoming nickel atoms. The baseplate 21 is rotated about the normal 107' to the extraction grid 38 during this evaporation to provide uniform coverage of the extraction grid 38 by the

15 sacrificial layer 107.

In a step 108, the emitter body 30A is formed of high resistivity material (Figure 6E) by deposition of a layer 109. In one embodiment, the emitter body 30A forms the bottom two-thirds of the overall height of the emitter 30'.

20 In one embodiment, the emitter body 30A is formed by co-evaporation of SiO together with Mn to provide the layer 109 and the emitter body 30A having 7-10 atomic percent Mn, as described in "Conduction Mechanisms In Co-Evaporated Mixed Mn/SiO$_x$ Thin Films" by S.Z.A. Zaidi, Jour. of Mater. Sci. 32, (1997), pp. 3349-3353. Other embodiments may employ

25 SiO formed as described in "Production of SiO$_2$ Films Over Large Substrate Area by Ion-Assisted Deposition of SiO With a Cold Cathode Source" by I.C. Stevenson, Soc. of Vac. Coaters, Proc. 36TH Annual Tech. Conf. (1993), pp. 88-93 or "Improvement of the ITO-P Interface in α-Si:H Solar Cells using a Thin SiO Intermediate Layer" by C. Nunes de Carvalho et al., Proc. MRS Spring

30 Symposium, Vol. 420 (1996), pp. 861-865, together with a co-deposited metal.

Other metals (*e.g.*, Cr, Au, Cu etc.) may be used to form cermet or cermet-like materials as described by Zaidi et al.

In a step 110, the emitter tips 30B are formed (Figure 6F) by deposition of a layer 111. In one embodiment, the layer 111 and the emitter tips
5 30B are formed by evaporation of one of the materials listed in Table I that are amenable to deposition by vacuum evaporation. TiN may be formed *in situ* by evaporation of a thin Ti film (*e.g.*, two hundred Angstroms or more) followed by rapid thermal annealing in a nitrogen-bearing atmosphere (*e.g.*, ammonia). In other embodiments, other materials may be sputtered or may be deposited by
10 chemical vapor deposition.

In one embodiment, silicon oxycarbide is employed as the emitter tips 30B in the step 110. A process for forming thin microcrystalline films of silicon oxycarbide is described in "Transport Properties of Doped Silicon Oxycarbide Microcrystalline Films Produced by Spatial Separation Techniques"
15 by R. Martins et al., Solar Energy Materials and Solar Cells 41/42 (1996), pp. 493-517. A diluent/reaction gas (*e.g.*, hydrogen) is introduced directly into a region where plasma ignition takes place. The mixed gases containing the species to be deposited are introduced close to the region where the growth process takes place, often a substrate heater. A bias grid is located between the
20 plasma ignition and the growth regions, spatially separating the plasma and growth regions.

Deposition parameters for producing doped microcrystalline $Si_x:C_y:O_z:H$ films may be defined by determining the hydrogen dilution rate and power density that lead to microcrystallization of the grown film. The power
25 density is typically less than 150 milliWatts per cm^3 for hydrogen dilution rates of 90%+, when the substrate temperature is about 250 °C and the gas flow is about 150 sccm. The composition of the films may then be varied by changing the partial pressure of oxygen during film growth to provide the desired characteristics.

In one embodiment, SiC is employed as the emitter tips 30B in the step 110. SiC films may be fabricated by chemical vapor deposition, sputtering, laser ablation, evaporation, molecular beam epitaxy or ion implantation of carbon into silicon. Vacuum annealing of silicon substrates is a method that may be used to provide SiC layers having thicknesses ranging from 20 to 30 nanometers, as described in "Localized Epitaxial Growth of Hexagonal and Cubic SiC Films on Si by Vacuum Annealing" by Luo et al., Appl. Phys. Lett. 69(7), (1996), pp. 916-918. This embodiment requires that the emitter tip 30B either be formed from or be coated with silicon. Prior to vacuum annealing, the emitters 30' are degreased with acetone and isopropyl alcohol in an ultrasonic bath for fifteen minutes, followed by cleaning in a solution of $H_2SO_4:H_2O_2$ (3:1) for fifteen minutes. A five minute rinse in deionized water then precedes etching with a 5% HF solution. The emitters 30' are blown dry using dry nitrogen and placed in the vacuum chamber and the chamber is pumped to a base pressure of $1\text{-}2\times10^{-6}$ Torr. The substrate is heated to 750 to 800 °C for half an hour to grow the microcrystalline SiC film.

In some embodiments, silicon is employed as the emitter tips 30B in the step 110. Methods for depositing high quality polycrystalline films of silicon on silicon dioxide substrates are given in "Growth of Polycrystalline Silicon at low Temperature on Hydrogenated Microcrystalline Silicon (μc-Si:H) Seed Layer" by Parks et al., Proceedings of the 1997 MRS Spring Symposium, Vol. 467 (1997), pp. 403-408, "Novel Plasma Control Method in PECVD for Preparing Microcrystalline Silicon" by Nishimiya et al., Proceedings of the 1997 MRS Spring Symposium, Vol. 467 (1997), pp. 397-401 and "Low Temperature (450°C) Poly-Si Thin Film Deposition on SiO_2 and Glass Using a Microcrystalline-Si Seed Layer" by D.M. Wolfe et al., Proceedings of the 1997 MRS Spring Symposium, Vol. 472 (1997), pp. 427-432. A process providing grain sizes of about 4 nm is described in "Amorphous and Microcrystalline Silicon Deposited by Low-Power Electron-Cyclotron Resonance Plasma-Enhanced Chemical-Vapor Deposition" by J.P. Conde et al., Jap. Jour. Appl.

Phys., Part I, Vol. 36, No. 1A (June 1997), pp. 38-49. Deposition conditions favoring small grain sizes for microcrystalline silicon include high hydrogen dilution, low temperature, low deposition pressure and low source-to-substrate separation.

5   Following the step 110, the sacrificial layer 107 is removed, along with those portions of the layers 109 and 111 that do not form parts of the emitters 30', in a step 112. In one embodiment, a nickel sacrificial layer 107 is removed using electrochemical etching of the nickel. Other conventional approaches for forming and later removing sacrificial layers 107 may also be

10 used when they are compatible with the processes of the steps 106-112. The process 100 then ends and further processing is carried out using conventional fabrication techniques.

    In one embodiment, emitters 30 formed from a single material are provided together with the porous silicon dioxide layer 34' formed as described

15 in conjunction with Figure 3 by performing the steps 102-106, performing a step 110' (not illustrated) of depositing a single material and then performing step 112. In this embodiment, the advantages of the porous silicon dioxide layer 34' may be provided together with conventional emitters 30.

    It will be appreciated that the porous silicon dioxide layer 34' may

20 be formed after formation of the emitters 30. In these embodiments, the emitters 30 may be conventionally formed before or after the step 77 of Figure 3. The steps 79-87 may, in some embodiments, follow the formation of the emitters 30 or 30'. In these embodiments, conventional chemical-mechanical polishing followed by etching of the porous silicon dioxide layer 34' results in a baseplate

25 21 (Figure 1) useful in field emission displays 10.

    Figure 7 is a simplified block diagram of a portion of a computer 120 including the field emission display 10, in accordance with the invention as described with reference to Figures 3-6 and associated text. The computer 120 includes a central processing unit 122 coupled via a bus 124 to a memory 126,

30 function circuitry 128, a user input interface 130 and the field emission display

10, according to embodiments of the present invention. The memory 126 may or may not include a memory management module (not illustrated) and does include ROM for storing instructions providing an operating system and a read-write memory for temporary storage of data. The processor 122 operates on data

5   from the memory 126 in response to input data from the user input interface 130 and displays results on the field emission display 10. The processor 122 also stores data in the read-write portion of the memory 126. Examples of systems where the computer 120 finds application include personal/portable computers, camcorders, televisions, automobile electronic systems, microwave ovens and

10   other home and industrial appliances.

Field emission displays 10 for such applications provide significant advantages over other types of displays, including reduced power consumption, improved range of viewing angles, better performance over a wider range of ambient lighting conditions and temperatures and higher speed with which the

15   display can respond. Field emission displays find application in most devices where, for example, liquid crystal displays find application.

Although the present invention has been described with reference to a preferred embodiment, the invention is not limited to this preferred embodiment. Rather, the invention is limited only by the appended claims,

20   which include within their scope all equivalent devices or methods which operate according to the principles of the invention as described.